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EXAMINER	
WONG, XAVIER S	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/627,486	KIM, YOUNG SUCK	
	Examiner	Art Unit	
	Xavier Szewai Wong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22nd October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Applicant's Amendment filed 22nd *October 2007* is acknowledged
- Claims **1**, **4**, **5**, **10**, **12**, **15**, **16** and **25** have been amended
- Claims **1-30** are still pending in the present application
- This action is made FINAL

Claim Objections

1. Objections on currently amended claims **4** and **12** have been withdrawn.

Claim Rejections - 35 USC § 112

2. 35 U.S.C § 112, *second* paragraph rejections on currently amended claims **1**, **5** and **15** have been withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims **16 – 20** are rejected under 35 U.S.C. 103(a) as being anticipated by the *applicant's admitted prior art* in view of **Andros et al** (**U.S Pat 4,868,558**).

Consider claims **16 – 20**, the applicant's admitted **prior art** fig. *1* shows a data redundancy system wherein a first active unit and second standby unit respectively comprising bridges (switches) *50A/50B* (paragraph *0005*), memories *10A/10B* for storing routing information (paragraph *0007*), and information from the first bridge (switch) *50A* stored in the first memory *10A* is transmitted to the second memory *10B* via one path the second bridge (switch) *50B* (paragraph *0009*). While the *applicant's admitted prior art* did not explicitly disclose *simultaneously* transferring the routing information to a second unit *while storing* the routing information in the first memory. **Andros et al** disclose a latch U54 can send (route) and store messages simultaneously once alerted of a failure in another latch (col. *26* ln. *27-33*; fig. *21A* U54 74HC646). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the concept and functionality of the latch as taught by **Andros et al** to the switch of the *applicant's admitted prior art* for efficient data transferring.

5. Claims **1** and **2** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aihara et al** (**U.S Pat 6,856,594 B1**).

Consider claim **1**, **Aihara et al** disclose an apparatus that performs channel routing of a (first) Node C and a (second) Node F in an ATM switching system wherein both nodes comprise a switch unit SW (fig. *2*) and cells (information) are routed/duplicated simultaneously (therefore, in real-time) (col. *1* ln. *42-51*; col *3* ln. *13-25*)

and therefore, eliminating a delay associated with a PCI-to-PCI board for routing information since **Aihara et al** did not mention a PCI board and that information is transmitted simultaneously from one node to the other node. The C switch routes routing information (in header address) to the F switch through line interfaces (col. *4* ln. *42-47*). While **Aihara et al** may not have explicitly mentioned the mirrored routing information is transferred along *one path*, the examiner takes official notice that it is well known in the art at the time the invention was made to have *one path* transferring mirrored information; for example, the *applicant's admitted prior art* shows in single-path between bridges *50A* (in first unit) and *50B* (in second unit) for preventing data loss (pg. *2*, paragraph *0005*).

Consider claim **2**, as applied to claim **1**, **Aihara et al** further disclose the first Node C switch comprises FIFO memory *31* to transfer information to second Node F (col. *4* ln. *47-50*; fig. *3*).

6. Claims **3**, **4**, **5**, **10**, **11**, **12**, **15**, **17 – 19**, **25 – 27** and **29** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aihara et al** (**U.S Pat 6,856,594 B1**) in view of **Tada** (**U.S Pat 6,487,169 B1**).

Consider claims **10** and **25**, **Aihara et al** disclose an apparatus, system and method that perform channel routing of a (first) Node C and a (second) Node F in an ATM switching system wherein both nodes comprise a switch unit SW (fig. *2*) and cells (information) are routed/duplicated (col. *1* ln. *42-51*; col *3* ln. *13-25*). The C switch loads a buffer with ATM cells with routing information (header address/virtual path id) and routes

the information to the F switch through line interfaces (col. *3* ln. *19-23*; col. *4* ln. *42-58*; fig. *2*). However, **Aihara et al** did not explicitly mention *loading a second memory in the second switch unit* with the information from the first switch unit or the routing information is transferred along *one path* from the first unit to the second unit. **Tada** discloses cells with routing information from an active (first) switch are loaded into buffer memories *6#1* of a standby (second) switch module *2#1* (col. *3* ln. *3-24*; col. *4* ln. *2-17/36-48*; claim *2*; fig. *1*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of loading routing information into a second memory of the second unit as taught by **Tada**, in the apparatus, system and method of **Aihara et al**, in order to minimize loss of cells. While **Aihara et al**, as modified by **Tada** and **Andros et al**, may not have explicitly mentioned the mirrored routing information is transferred along *one path*, the examiner takes official notice that it is well known in the art at the time the invention was made to have *one path* transferring mirrored information; for example, the *applicant's admitted prior art* shows in single-path between bridges *50A* (in first unit) and *50B* (in second unit) for preventing data loss (pg. *2*, paragraph *0005*).

Consider claim **3**, and as applied to claim **2**, **Aihara et al** disclose the claimed invention except explicitly showing *the storing of routing information in a second memory of the second unit*. **Tada** discloses cells with routing information are stored in buffer memories *6#1* of a (second) standby switch module *2#1* (col. *3* ln. *3-24*; col. *4* ln. *2-17*; claim *2*; fig. *1*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of storing routing information in a second memory of the

second unit as taught by **Tada**, in the apparatus and system of **Aihara et al**, in order to minimize loss of cells.

Consider claims **4** and **5**, and as applied to claims **2** and **3**, **Aihara et al** disclose the claimed invention except routing information being stored in a second memory; both the first and second switching unit prevents signal transmission to the second unit and memory. **Tada** further discloses that every active (first) or standby (second) switch operation is performed synchronously (col. *3* ln. *21-23*); therefore, no interruption during transmission translates to no signal is transmitted from either first or second switches. Furthermore, **Tada** mentions as the active (first) switch reads out/transmits all its cells to the standby (second) switch (from a full load) after a time tip and cells are written into a buffer in the standby switch (col. *4* ln. *18-49*); therefore, no signal interrupts the buffer memory while transmission is in progress. It would have been obvious to one of ordinary skill in the art to incorporate the teachings by **Tada**, in the apparatus and system of **Aihara et al**, in order to minimize loss of cells.

Consider claims **11** and **12**, as applied to claim **10**, are rejected in the same grounds as claims **4** and **5.**

Consider claim **15**, and as applied to claim **10**, is rejected in the same grounds as claims **8** and **9**.

Consider claims **26 – 27**, as applied to claims **25 – 26**, **Aihara et al**, as modified by **Tada**, illustrate in fig. *2* that Node C and Node F both comprise switch units SW.

Consider claim **29**, and as applied to claim **25**, **Aihara et al**, as modified by **Tada**, further illustrate in fig. *2*, a 2:1 multiplexer (MUX *3-1*) with 2 input terminals, 1

output terminal, and 1 control terminal (item *4*) responsive to a select signal (col. *4* ln. *32-34*; col. *5* ln. *40-42*).

7. Claims **6** and **13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aihara et al** (**U.S Pat 6,856,594 B1**) in view of in view of **Tada** (**U.S Pat 6,487,169 B1**), as applied to claims **5** and **12**, and in further view of **Kamiya et al** (**U.S Pat 6,493,593 B1**).

Consider claims **6** and **13**, and as applied to claims **5** and **12**, **Aihara et al** as modified by **Tada** disclose the claimed invention except the second switching unit prevents data from being loaded from the second memory. **Kamiya et al** disclose a switch (first or second) that is capable of preventing data being loaded into a memory (col. *28* ln. *66-67*; col. *29* ln. *1-4*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of a (second) switching unit prevents data from being loaded from a (second) memory as taught by **Kamiya et al**, in the apparatus of **Aihara et al** as modified by **Tada**, for distinguishing the non-related objects from related objects to be reloaded into the memory.

8. Claim **7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Aihara et al** (**U.S Pat 6,856,594 B1**) in view of **Kicklighter** (**U.S Pat 6,005,841**).

Consider claim **7**, and as applied to claim **1**, **Aihara et al** disclose the claimed invention except mentioning that the first and second switches are programmable. **Kicklighter** discloses an active (first) and standby (second) programmable switches

redundancy arrangement (col. *1* ln *16-22*; claim *7*; fig. *1* items *44a/b*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of programmable switches as taught by **Kicklighter**, in the apparatus of **Aihara et al**, for flexibility.

9. Claims **8** and **9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aihara et al** (**U.S Pat 6,856,594 B1**) in view of in view of **Tada** (**U.S Pat 6,487,169 B1**), as applied to claim **7**, and in further view of **Kicklighter** (**U.S Pat 6,005,841**).

Consider claims **8** and **9**, and as applied to claims **7** and **10**, **Aihara et al** disclose the claimed invention except explicitly showing the first and second switches are structural and functional equivalents. **Tada** shows both active (first) and standby (second) switch modules are structural equivalent according to fig. *1*; and functional equivalent as mentioned are interchangeable and executed in the same manner (col. *2* ln. *47-65*; col. *15* ln. *5-6*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of first and second switches are structural and functional equivalents as taught by **Tada**, in the apparatus of **Aihara et al**, for scalability.

10. Claim **14** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Aihara et al** (**U.S Pat 6,856,594 B1**) in view of **Tada** (**U.S Pat 6,487,169 B1**), and as applied to claim **10**, and in further view of **Kicklighter** (**U.S Pat 6,005,841**).

Consider claim **14**, and as applied to claim **10**, is rejected in the same grounds as claim **7**.

11. Claims **16 – 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aihara et al** (**U.S Pat 6,856,594 B1**) in view of **Tada** (**U.S Pat 6,487,169 B1**) and in further view of **Andros et al** (**U.S Pat 4,868,558**).

Consider claim **16, Aihara et al** disclose an apparatus, system and method that perform channel routing of a (first) Node C and a (second) Node F in an ATM switching system wherein both nodes comprise a switch unit SW (fig. *2*) and cells (information) are routed/duplicated (col. *1* ln. *42-51*; col *3* ln. *13-25*). The C switch loads a buffer with ATM cells with routing information (header address/virtual path id) and routes the information to the F switch through line interfaces (col. *3* ln. *19-23*; col. *4* ln. *42-58*; fig. *2*). However, **Aihara et al** did not explicitly mention *loading a second memory in the second switch unit* with the information from the first switch unit or *simultaneously routing* information to the second unit along *one path* and *storing* the information the first unit. **Tada** discloses cells with routing information from an active (first) switch are loaded into buffer memories *6#1* of a standby (second) switch module *2#1* (col. *3* ln. *3-24*; col. *4* ln. *2-17/36-48*; claim *2*; fig. *1*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of loading routing information into a second memory of the second unit as taught by **Tada**, in the apparatus, system and method of **Aihara et al**, in order to minimize loss of cells. In addition, **Andros et al** disclose a latch U54 can send (route) and store messages simultaneously once alerted of a failure in another latch (col. *26* ln. *27-33*; fig. *21A* U54 74HC646). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the concept and functionality of the latch as taught by **Andros et al** to the switch of the

Aihara et al, as modified by **Tada**, for efficient data transferring. While **Aihara et al**, as modified by **Tada** and **Andros et al**, may not have explicitly mentioned the mirrored routing information is transferred along *one path*, the examiner takes official notice that it is well known in the art at the time the invention was made to have *one path* transferring mirrored information; for example, the *applicant's admitted prior art* shows in single-path between bridges *50A* (in first unit) and *50B* (in second unit) for preventing data loss (pg. *2*, paragraph *0005*).

Consider claims **17 – 19**, as applied to claims **16 – 18**, **Aihara et al**, as modified by **Tada** and **Andros et al**, illustrate in fig. *2* that Node C and Node F both comprise switch units SW.

Consider claim **20**, and as applied to claim **19**, **Aihara et al**, as modified by **Tada** and **Andros et al**, disclose the claimed invention except explicitly showing *the storing of routing information in a second memory of the second unit*. **Tada** discloses cells with routing information are stored in buffer memories *6#1* of a (second) standby switch module *2#1* (col. *3* ln. *3-24*; col. *4* ln. *2-17*; claim *2*; fig. *1*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of storing routing information in a second memory of the second unit as taught by **Tada**, in the apparatus and system of **Aihara et al** as modified by **Andros et** al, in order to minimize loss of cells.

12. Claims **21 – 24**, **28** and **30** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aihara et al** (**U.S Pat 6,856,594 B1**) in view of in view of **Tada** (**U.S**

Pat 6,487,169 B1) and **Andros et al** (**U.S Pat 4,868,558**), as applied to claims **16**, **21**, **25** and **29**, and in further view of **Asfour** (**U.S Pat 5,182,801**).

Consider claims **21** and **28**, and as applied to claims **16** and **25**, **Aihara et al**, as modified by **Tada** and **Andros et al**, disclose the claimed invention including a multiplexer. However, **Aihara et al** as modified by **Tada** and **Andros et al** did not disclose *a tri-state buffer in communication with the multiplexer*; wherein the first switching unit is configured to *connect a plurality of external devices to route signal inputted from a first device to a second device according to control information*. **Asfour** illustrates in fig. *4* that a (first) switch *40* with a multiplexer (MUX *81* or *82*) in communication with a tri-state buffer (*86a* or *86b*); and in fig. *1* the switch unit *40* is coupled to external devices *10* & *11,* which are connected to each other; wherein (first) device *10* may send a request to (second) device *11* and a control logic *50* as the control arbitrates a decision (col. *4* ln. *4-10*; col. *8* ln. *4-19*). It would have been obvious to one of ordinary skill in the art to incorporate the above teachings by **Asfour**, in the system and method of **Aihara et al** as modified by **Tada** and **Andros et al**, for data transfers between devices.

Consider claim **22**, and as applied to claim **21**, is rejected in the same grounds as claim **29**.

Consider claims **23**, **24** and **30**, and as applied to claims **22** and **29**, **Aihara et al** as modified by **Tada** and **Andros et al** disclose the claimed invention except explicitly mentioning a multiplexer outputting a first signal when a select signal is in a first state; and outputting a second signal when the select signal is in a second state; wherein

when the select signal is a first value, the tri-state buffer is in output-enable state, and when select signal is a second value, the tri-state buffer is in output-disable state. **Asfour** discloses control signals (through decode logic *49* → select signal; line *85a* in fig. *4*) are applied to the multiplexer *82* and tri-state output buffer *87a* to route connection to any (therefore; may be in 1.) connected state; or 2.) not-connected state) memory ports (col. *6* ln. *41-46*). Therefore, when a (first) signal is output from the multiplexer, the tri-state buffer can accordingly be in a first (output-enable/connected or output-disable/not-connected) state; when a (second) signal is output from the multiplexer, the tri-state buffer can accordingly be in a second (output-disable/not-connected or output-enable/connected) state. It would have been obvious to one of ordinary skill in the art to incorporate the teachings above by **Asfour**, in the system and method of **Aihara et al** as modified by **Tada** and **Andros et al**, for memory management purposes.

Response to Arguments

13. Applicant's arguments with respect to claims **1**, **16** and **25** have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, this action is made FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is 571-270-1780. The examiner can normally be reached on Monday through Friday 8:30 am - 6:00 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Xavier Szewai Wong
X.S.W / x.s.w
15th November 2007

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